AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A thin film transistor comprising:

a buffer layer formed on a substrate;

an activation layer formed on said buffer layer; and

a gate insulation layer formed on said substrate including said activation layer,

with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and said step being a half or less of the thickness sum of said activation layer and gate insulation layer.

2. (Original) The thin film transistor according to claim 1, wherein said buffer layer has a step to such a degree that thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

3. (Currently Amended) The thin film transistor according to claim 1, wherein a thickness of the gate insulation layer is at least 400 Å when [[the]] a thickness of [[SPC]] solid-phase crystallization polysilicon is 300 Å and step is 350 Å in the activation layer.

4. (Currently Amended) The thin film transistor according to claim 1, wherein thickness of the gate insulation layer is at least 1,000 Å when [[the]] a thickness of [[ELA]] excimer laser annealing polysilicon is 500 Å and step is 750 Å in the activation layer.

5. (Currently Amended) The thin film transistor according to claim 2, wherein a thickness of the gate insulation layer is 400 Å or more when [[the]] a thickness of [[SPC]] solid-phase crystallization polysilicon is 300 Å and step is 350 Å in the activation layer.

6. (Currently Amended) The thin film transistor according to claim 2, wherein thickness of the gate insulation layer is 1,000 Å or more when [[the]] a thickness of [[ELA]] excimer laser annealing polysilicon is 500 Å and step is 750 Å in the activation layer.

7. (Withdrawn) A method for fabricating said thin film transistor of claim 1, comprising the steps of:

depositing an amorphous silicon layer on a substrate equipped with buffer layer;

forming a polycrystalline silicon layer by crystallizing said amorphous silicon layer;

forming an activation layer by etching said polycrystalline silicon layer;

treating the surface of said activation layer; and

depositing a gate insulation layer on said substrate,

with etching time being controlled in said activation layer forming process and activation layer surface treatment process so that step between a lower part of gate in the buffer layer and a part

except the lower part of said gate has a step value corresponding to a half or less of the thickness sum of said activation layer and gate insulation layer.

8. (Withdrawn) The method for fabricating a thin film transistor according to claim 7, wherein the etching time is controlled so that said buffer layer has a step to such a degree that thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

9. (Withdrawn) The method for fabricating a thin film transistor according to claim 7, wherein the etching time is controlled to accommodate said buffer layer having a step corresponding to a half or less of the thickness sum of the activation layer and gate insulation layer.

10. (Withdrawn) The method for fabricating a thin film transistor according to claim 9, wherein the etching time is controlled so that said buffer layer has a step to such a degree that thickness of said gate insulation layer is not changed on said side wall of said buffer layer.

11. (Currently Amended) The method for fabricating a thin film transistor according to claim 7, wherein a thickness of said gate insulation layer is 400 Å or more when the thickness of [[SPC]] solid-phase crystallization polysilicon is 300 Å and step is 350 Å in said activation layer.

12. (Currently Amended) The method for fabricating a thin film transistor according to claim 7, wherein thickness of said gate insulation layer is 1,000 Å or more when the thickness of [[ELA]]

excimer laser annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

13. (Original) A thin film transistor, comprising:

a buffer layer;

an activation layer formed on said buffer layer; and

a gate insulation layer formed on said buffer layer and said activation layer,

with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and said step being up to a half of the thickness sum of said activation layer and gate insulation layer.

14. (Original) The thin film transistor according to claim 13, with said step being controlled according to said gate insulation layer being deposited to an even thickness on a side wall of said activation layer.

15. (Currently Amended) The thin film transistor according to claim 13, with a thickness of said gate insulation layer being at least 400 Å when [[the]] a thickness of [[SPC]] solid-phase crystallization polysilicon is 300 Å and step is 350 Å in said activation layer.

16. (Currently Amended) The thin film transistor according to claim 13, with a thickness of said gate insulation layer being at least 1,000 Å when [[the]] a thickness of [[ELA]] excimer laser annealing polysilicon is 500 Å and step is 750 Å in said activation layer.

17. (Withdrawn) A method for fabricating a thin film transistor including a buffer layer, an activation layer formed on said buffer layer, and a gate insulation layer formed on said buffer layer and said activation layer, with said buffer layer having a step formed between a lower part of said activation layer and a part except said lower part of said activation layer, and said step being up to a half of the thickness sum of said activation layer and gate insulation layer, said thin film transistor comprising:

forming a polycrystalline silicon layer;

forming an activation layer by etching said polycrystalline silicon layer;

treating the surface of said activation layer; and

depositing a gate insulation layer on said substrate,

with etching time being controlled in the activation layer forming process and activation layer surface treatment process to accommodate a step between a lower part of a gate in said buffer layer and a part except the lower part of said gate having a step value corresponding up to a half of the thickness sum of said activation layer and gate insulation layer.

18. (Withdrawn) The method for fabricating a thin film transistor according to claim 17, wherein the etching time is controlled to accommodate said buffer layer including the step to such a degree where said gate insulation layer is deposited to an even thickness on a side wall of said activation layer.

19. (Withdrawn) The method for fabricating a thin film transistor according to claim 17, wherein the etching time is controlled to accommodate said buffer layer having a step corresponding up to half of the thickness sum of the activation layer and gate insulation layer.

20. (Currently Amended) The method for fabricating a thin film transistor according to claim 17, wherein a thickness of said gate insulation layer is at least 400 Å when the thickness of [[SPC]] solid-phase crystallization polysilicon is 300 Å and the step is 350 Å in the activation layer or the thickness of said gate insulation layer is at least 1,000 Å when the thickness of [[ELA]] excimer laser annealing polysilicon is 500 Å and the step is 750 Å in said activation layer.